WHAT IS CLAIMED IS:

1. A switch comprising:

a plurality of ports operable to communicate packets;

a switch fabric operable to transport received packets between the ports;

a plurality of memory banks logically divided into a plurality of rows, wherein each of the rows comprises a storage location from each of the memory banks, each of the storage locations capable of maintaining a routing entry;

an overflow buffer comprising a plurality of overflow storage locations each capable of maintaining a routing entry; and

a memory control module operable to receive a memory access request from one of the ports, to determine a particular one of the rows based on an address indicated by the memory access request, and to access the indicated row and the overflow buffer to perform a memory access operation.

2 The switch of Claim 1, wherein the memory access request requests a lookup operation, and the memory control module is further operable to perform the memory access operation by:

receiving potential routing entries from the indicated row and from the overflow buffer;

comparing the address against each of the potential routing entries; and

if the address matches one of the potential routing entries, to return routing information indicated by the matching one of the potential routing entries.

3 The switch of Claim 1, wherein the memory access request requests a learn operation specifying routing information, and the memory control module is further operable to perform the memory access operation by:

determining that the indicated row has valid routing entries in every one of the storage locations in the indicated row;

determine an available one of the overflow storage locations; and

write the address and the routing information into the available one of the overflow storage locations.

4. The switch of Claim 1, wherein the memory control module comprises:

an arbitration module operable to receive lookup requests and learn requests from the ports and to schedule a series of memory access operations based upon the lookup requests and the learn requests; and

a memory access module operable, for each of the series of memory access operations, to determine a hash key from an address indicated by the one of the series of memory access operations, wherein the hash key indicates a particular one of the rows, and to access the overflow buffer and the particular row indicated by the hash key.

5 The switch of Claim 4, wherein the arbitration module schedules memory access operations to service any outstanding lookup requests before scheduling memory access operations to service any outstanding learn requests.

6. The switch of Claim 4, wherein to service a learn request, the arbitration module is operable to:

schedule first memory access operations that include a read operation indicating a source address from the learn request;

determine whether the read operation detected a miss in the memory banks and the overflow buffer; and

if the miss is detected, to schedule second memory access operations that include a write operation indicating a source address and a port mapping from the learn request.

7. The switch of Claim 6, wherein the arbitration module is further operable to insure that the first memory access operations do not include any write operations.

8. The switch of Claim 1, wherein the overflow buffer comprises a plurality of memory elements.

9. The switch of Claim 8, wherein each of the memory elements corresponds to a plurality of the rows, and the memory control module is further operable to access the indicated row and the overflow buffer to perform the memory access operation by accessing the indicated row and the one or more ones of the memory elements corresponding to the indicated row.

10. A method for performing routing table operations comprising:

monitoring for lookup requests and learn requests received from any of a plurality of ports;

detecting a lookup request comprising a destination address;

determining a hash key based on the destination address;

accessing a memory module using the hash key, wherein the memory module comprises a plurality of memory banks logically divided into a plurality of rows, wherein each of the rows comprises a storage location from each of the memory banks, each of the storage locations capable of maintaining a routing entry, wherein the hash key indicates one of the row;

accessing an overflow buffer comprising a plurality of overflow storage locations each capable of maintaining a routing entry;

determining whether one of the entries from the indicated row or from the overflow buffer includes address information matching the destination address;

if the indicated row or the overflow buffer includes a matching entry, returning routing information from the matching entry, the routing information identifying one or more of the ports.

11. The method of Claim 10, further comprising:

detecting a learn request that identifies a source address and routing information;

determining a second hash key based on the source address;

accessing the memory module using the second hash key, wherein the second hash key indicates a second one of the rows.

12. The method of Claim 11, further comprising insuring that none of the memory banks perform a write operation while accessing the memory module using the second hash key.

13. The method of Claim 11, further comprising:

determining whether one of the entries from the second indicated row includes address information matching the source address;

if none of the entries match, determining whether the second indicated row includes an available storage location; and

if the second indicated row includes an available storage location, writing the source address and the routing information to the available storage location.

14. The method of Claim 11, further comprising:

determining whether one of the entries from the second indicated row includes address information matching the source address;

if none of the entries match, determining whether the second indicated row includes an available storage location; and

if the second indicated row does not include an available storage location, determining an available overflow storage location and writing the source address and the routing information to the available overflow storage location.

15 The method of Claim 10, further comprising servicing any outstanding lookup requests prior to servicing any outstanding learn requests.

16. The method of Claim 10, further comprising determining that the destination address is a multicast address and, in response, insuring that none of the memory banks perform a write operation while accessing the memory module using the hash key.

17. The method of Claim 10, further comprising performing a write operation while accessing the memory module using the hash key, the write operation indicating a particular one of the storage locations within a selected one of the memory banks, wherein accessing the memory module using the hash key reads the entries from the indicated row in all of the memory banks except for the memory bank indicated in the write operation.

18. A switch comprising:

means for monitoring for lookup requests and learn requests received from any of a plurality of ports;

means for detecting a lookup request comprising a destination address;

means for determining a hash key based on the destination address;

means for accessing a memory module using the hash key, wherein the memory module comprises a plurality of memory banks logically divided into a plurality of rows, wherein each of the rows comprises a storage location from each of the memory banks, each of the storage locations capable of maintaining a routing entry, wherein the hash key indicates one of the row;

means for accessing an overflow buffer comprising a plurality of overflow storage locations each capable of maintaining a routing entry;

means for determining whether one of the entries from the indicated row or from the overflow buffer includes address information matching the destination address;

means for, if the indicated row or the overflow buffer includes a matching entry, returning routing information from the matching entry, the routing information identifying one or more of the ports.

19. The switch of Claim 18, further comprising:

means for detecting a learn request that identifies a source address and routing information;

means for determining a second hash key based on the source address;

means for accessing the memory module using the second hash key, wherein the second hash key indicates a second one of the rows.

20. The switch of Claim 19, further comprising means for insuring that none of the memory banks perform a write operation while accessing the memory module using the second hash key.

21. The switch of Claim 19, further comprising:

means for determining whether one of the entries from the second indicated row includes address information matching the source address;

means for, if none of the entries match, determining whether the second indicated row includes an available storage location; and

means for, if the second indicated row includes an available storage location, writing the source address and the routing information to the available storage location.

22. The switch of Claim 19, further comprising:

means for determining whether one of the entries from the second indicated row includes address information matching the source address;

means for, if none of the entries match, determining whether the second indicated row includes an available storage location; and

means for, if the second indicated row does not include an available storage location, determining an available overflow storage location and writing the source address and the routing information to the available overflow storage location.